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Signature

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231

RE: *U.S. Patent Application Entitled: LOW NOISE LOGIC GATE – Daren Allee (2000.000900/TT2273)*

Sir:

Transmitted herewith for filing are:

(1) 14-page patent specification with 9 claims and an abstract (also Figures 1-4 on 4 sheets);
(2) Declaration;
(3) Power of Attorney; and
(4) Assignment and Assignment Cover Sheet.

All correspondence, notices, official letters and other communications should be directed to Terry D. Morgan, Williams, Morgan & Amerson, P.C., 7676 Hillmont, Suite 250, Houston, TX 77040, and all telephone calls should be directed to Terry D. Morgan at (713) 934-4050.

EL332807437US

The Assistant Commissioner is authorized to deduct the amount of the total filing fee (listed below) from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/TT2273.

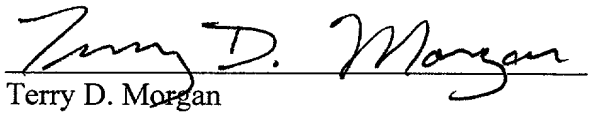
FILING FEE CALCULATION

FOR		Small Entity	Large Entity
Total Claims	17 - 20 = 0	x $9 = $	or x $18 = $ 0.00
Independent Claims	2 - 3 = 0	x $39 = $	or x $78 = $ 0.00
Multiple Dependent Claim(s)		+ $130 = $	or + $260 = $ 0.00
Basic Fee:		+ $380 = $	or + $760 = $ 760.00
Assignment Recording Fee:	($40 per assignee)	+ = $	+ = $ 40.00
TOTAL FILING FEES		**$ 0.00**	**$ 800.00**

Pursuant to 37 C.F.R. § 1.10 the Applicants request the Patent and Trademark Office to accept this application and accord a serial number and filing date as of the date this application is deposited with the U.S. Postal Service for Express Mail.

Please date stamp and return the enclosed postcards to evidence receipt of these materials.

Respectfully submitted,



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Enclosures
cc: Ms. Laura K. Fenton (w/enc.)

2000.000900
TT2273

Application for United States Letters Patent

for

LOW NOISE LOGIC GATE

By

Daren Allee

EXPRESS MAIL MAILING LABEL
NUMBER: EL332807437US
DATE OF DEPOSIT : Septemer 20, 1999
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LOW NOISE LOGIC GATE

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

This invention relates generally to a logic gate, and, more particularly, to a low-noise, logic gate used, for example, in a voltage controlled oscillator.

2. DESCRIPTION OF THE RELATED ART

In the field of wireless telecommunications, noise problems are a significant problem. For example, in cordless telephone sets, a handset and base communicate over a radio link instead of through a wire. Noise may reduce the useable range, or more problematic, even eliminate proper operation by interfering with the radio link between the handset and the base of the telephone set.

Some noise is environmental in nature. That is, some noise comes from the environment in which the telephone set is located. For example, other electronic equipment operating near the telephone set can produce EMI (electromagnetic interference) that causes noise to be impressed onto the circuitry of the telephone set. Shielding the telephone set can reduce some environmental noise, however, in applications such as cordless telephones, shielding may not be entirely effective. In fact, cordless telephones have been recently designed to operate in a frequency range (~900MHz) that should normally be outside the range of noise produced by many home appliances. That is, the radio signals delivered between the handset and the telephone base are carried by a 900MHz electromagnetic signal. Most home appliances do not produce EMI in this frequency range.

Another type of noise that can impair voice signal clarity arises from inside the telephone set. That is, the telephone set may produce noise internally that is impressed on the radio signal. Two examples are device noise and switching noise. Oscillators are commonly used to produce the ~900 MHz carrier signal used in cordless telephones. Any noise introduced by the oscillator will ultimately be delivered over the radio link, interfering with the proper operation.

The present invention is directed to overcoming, or at least reducing the effects of, one or more of the problems set forth above.

SUMMARY OF THE INVENTION

In one aspect of the present invention, a logic gate is provided. A low noise current source is coupled between a first terminal of a voltage supply and an output terminal. The low noise current source is capable of delivering a preselected voltage signal to the output terminal having a magnitude responsive to a first control signal relatively independent of the magnitude of the voltage on said first terminal of said voltage supply. At least one switching element is coupled between the output terminal and a second terminal of the voltage supply. The switching element is capable of coupling the output terminal to the second terminal of the voltage supply in response to receiving a second control signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figure 1 illustrates an electrical schematic of one embodiment of a voltage controlled oscillator;

Figure 2 illustrates an electrical schematic of one embodiment of a comparator circuit of the voltage controlled oscillator of Figure 1;

Figure 3 illustrates an electrical schematic of one embodiment of a delay circuit of the voltage controlled oscillator of Figure 1; and

Figure 4 illustrates a timing diagram of waveforms corresponding to various nodes of the voltage controlled oscillator of Figure 1.

While the invention is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and are described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

Turning now to the drawings, and in particular, to Figure 1, a schematic of one embodiment of a voltage controlled oscillator 10 is shown. The voltage controlled oscillator 10 includes first and second edge delay circuits 12, 14. The edge delay circuits 12, 14 have output terminals respectively connected to first and second comparator circuits 16, 18. The comparator circuits 16, 18 are respectively formed from an AND gate 20, 24 having its output terminal coupled to an input terminal of a NOR gate 22, 26. The output terminals of the comparator circuits 16, 18 are coupled to complementary phase output terminals 30, 28. The complementary phase output terminals 28, 30 are also coupled to the input terminals of the edge delay circuits 12, 14 and to one of the input terminals of the NOR gates 22, 26.

Oscillation of the VCO 10 is ensured by a pair of NOR gates 34, 36. Each of the NOR gates 34, 36 has a first input terminal coupled to the complementary phase output terminals 28, 30. Output terminals of the NOR gates 34, 36 are coupled to a second input

terminal of the AND gates 20, 24, respectively. The output terminals of the NOR gates 34, 36 are also cross coupled to a second input terminal of the NOR gates 36, 34, respectively.

The frequency at which the VCO 10 oscillates is effected by a control input terminal 32 coupled to a control input terminal of the NOR gates 22, 26 and the edge delay circuits 12, 14. An analog voltage placed on the control input terminal 32 affects the rate at which the edge delay circuits 12, 14 charge to a logically high voltage level and the level at which the comparator circuits 16, 18 switch between a logically low level and a logically high level. Thus, a single control voltage is advantageously used in multiple components to control the frequency of the VCO 10.

The edge delay circuits 12, 14 are capable of pulling their output terminals to a logically low level relatively quickly, whereas the transition to a logically high level occurs substantially slower. Operation of the VCO 10 may be understood by reference to the timing diagram of Figure 4. The timing diagram of Figure 4 includes representations of various terminals of Figure 1. For example, the waveforms at the output terminals of the edge delay circuits 12, 14 are represented by the lines labeled 50 and 51, respectively. Likewise, the waveforms at the output terminals of the NOR gates 34, 36 are represented by the lines labeled 52 and 53, respectively. The waveforms present at the complementary phase output terminals 30, 28 are represented by the lines labeled 55, 54, respectively.

For purposes of describing the operation of the VCO 10, assume an initial condition where the output 54 of the complementary phase output terminal 28 is at a logically high level and just beginning a transition to a logically low level (point A on line 54). As the

output 54 transitions to a logically low level, it causes the output 50 of the edge delay circuit 12 to begin a relatively slow transition to a logically high level. At the same time, the logically low level at the output 54, through the comparator circuit 16 causes the output 55 to rapidly transition to a logically high level. The output 55 will remain at the logically high level until the relatively slow charging output 50 reaches the logically high level. Once the output 50 reaches the logically high level, the output 55 of the comparator circuit 16 rapidly transitions to a logically low level. The logically low level of the output 55 causes the output 51 of the edge delay circuit 14 to begin a relatively slow transition to a logically high level, and to immediately transition the output 54 back to a logically high level. Once the output 51 reaches the logically high level, the output 54 of the comparator circuit 18 rapidly transitions to a logically low level, repeating the operation.

It should be appreciated that the VCO 10 does not exhibit a hysteresis effect, which eliminates regenerative feedback, and thus, noise sensitivity. It should also be appreciated that the logic circuitry used in the VCO 10 could be readily modified to provide a relatively fast high-to-low transition and a relatively slow low-to-high transition by, *inter alia*, replacing the NOR gates 22, 26 with NAND gates (not shown) and the AND gates 20, 24 with OR gates (not shown).

Turning now to Figure 2, an electrical schematic of one embodiment of the comparator circuit 16 of Figure 1 is shown. A low noise current source 60 is coupled to a power supply 62. The current source 60 is formed from a serially connected resistor 64 and a P-intrinsic transistor 66. The gate of the transistor 66 is coupled to the control input terminal 32, such that an analog voltage placed on the control input terminal 32 affects the magnitude

of the current supplied. A pair of transistors 68, 70 are gate-to-drain coupled in series between system ground and the complementary phase output terminal 30. The transistors 68, 70 clamp the voltage appearing at the complementary phase output terminal 30 to about a two threshold voltage drop. This keeps the current source 60 working despite variations in the supply voltage.

The AND gate 20 of the comparator circuit 16 is formed by a pair of transistors 72, 74 serially coupled between the complementary phase output terminal 30 and system ground. The gates of the transistors 72, 74 are coupled to the output terminals 71a, 71b of the edge delay circuit 12 and the NOR gate 34. Thus, when the gates of the transistors 72, 74 are both logically high, then both conduct current, pulling the complementary phase output terminal 30 toward system ground. When neither, or only one, of the gates of the transistors 72, 74 are logically high, then the current source 60 supplies current to charge the complementary output terminal 30.

The NOR gate 22 of the comparator circuit 16 is formed by the AND gate 20 connected in parallel with a transistor 76. The gate of the transistor 76 is coupled to the complementary phase output terminal 28 through a terminal 77. Thus, when the complementary phase output terminal 28 reaches a logically high level, the transistor 76 conducts, pulling the complementary phase output terminal 30 to a logically low level. Likewise, when both input terminals of the AND gate 20 reaches a logically high level, the transistors 72, 74 conduct, pulling the complementary phase output terminal 30 to a logically low level.

The current source 60 is resistant to noise for at least two reasons. First, current sources in general are inherently resistant to variations in their supply voltage. Thus, variations in the magnitude of the voltage delivered by the power supply 62 has little or no impact on the current level delivered to the output terminal 30 as long as the input terminal 32 is varying with the voltage supply 62. Second, the resistor 64 and P-intrinsic transistor 66 are low noise devices as compared to standard MOS devices. The P-intrinsic transistor 66 is formed using only a single injected dopant. Ordinarily, MOS transistors (non-intrinsic) are formed using multiple dopings. Often, three doping steps are used to form a conventional transistor. As doping levels increase in a transistor, a phenomena known as flicker noise becomes more significant. Flicker noise, induced by a conventional transistor, can show up in the oscillator signal and ultimately reduce the performance of the telephone set. In the instant invention, less doping means less noise and better performance.

The low noise current source 60 generally performs well throughout most of its expected range of operation. However, as the voltage appearing at the terminal 30 approaches a power supply rail, such as system voltage, performance lags. Accordingly, the clamping transistors 68, 70 have been introduced to clamp the voltage to a stable level as the voltage at the terminal 30 approaches the rail.

Turning now to Figure 3, an electrical schematic of one embodiment of the edge delay circuit 12 of Figure 1 is shown. A low noise current source 80 (similar to the current source 60 of Figure 2) is coupled to the power supply 62. The current source 80 is formed from a serially connected resistor 82 and a P-intrinsic transistor 84. The gate of the transistor 84 is coupled to the control input terminal 32, such that an analog voltage placed on the control

input terminal 32 affects the magnitude of the current supplied. A capacitor 86 is serially coupled between the current source 80 and system ground, such that the current source 80 is capable of charging the capacitor 86 at a rate determined by the magnitude of the current supplied by the current source 80. That is, the higher the voltage delta at the control input terminal 32 relative to Vcc, the more current that is supplied, and the faster the capacitor 86 charges.

A transistor 88 is coupled in parallel with the capacitor 86, and has its gate coupled to the complementary phase output terminal 28. Thus, when the complementary phase output terminal 28 is at a logically high level, the transistor 88 conducts, quickly pulling the complementary phase output terminal 28 to a logically low voltage level. On the other hand, when the complementary phase output terminal 28 is at a logically low level, the transistor 88 does not conduct, and the capacitor is relatively slowly charged toward a logically high voltage level by the current source 80.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

CLAIMS

WHAT IS CLAIMED:

1. A logic gate, comprising:

a low noise current source coupled between a first terminal of a voltage supply and an output terminal, said low noise current source being capable of delivering a preselected voltage signal to said output terminal having a magnitude responsive to a first control signal relatively independent of the magnitude of the voltage on said first terminal of said voltage supply; and

at least one switching element coupled between the output terminal and a second terminal of the voltage supply, said switching element being capable of coupling said output terminal to said second terminal of said voltage supply in response to receiving a control signal.

2. A logic gate, as set forth in claim 1, wherein said low noise current source includes a transistor and a resistor serially coupled between the first terminal of the voltage supply and the output terminal, the transistor having a gate capable of receiving the first control signal.

3. A logic gate, as set forth in claim 2, wherein said transistor is an intrinsic transistor.

4. A logic gate, as set forth in claim 1, including a capacitor coupled between the output terminal and the second terminal of the voltage supply.

5. A logic gate, as set forth in claim 1, including at least one clamping diode coupled between the output terminal and the second terminal of the voltage supply.

6. A logic gate, comprising:

a low noise current source coupled between a first terminal of a voltage supply and an output terminal, said low noise current source including an intrinsic transistor being capable of delivering a preselected voltage signal to said output terminal having a magnitude responsive to a first control signal relatively independent of the magnitude of the voltage on said first terminal of said voltage supply; and

at least one switching element coupled between the output terminal and a second terminal of the voltage supply, said switching element being capable of coupling said output terminal to said second terminal of said voltage supply in response to receiving a control signal.

7. A logic gate, as set forth in claim 6, wherein said low noise current source includes a resistor serially coupled with said intrinsic transistor between the first terminal of the voltage supply and the output terminal, the intrinsic transistor having a gate capable of receiving the first control signal.

8. A logic gate, as set forth in claim 6, including a capacitor coupled between the output terminal and the second terminal of the voltage supply.

9. A logic gate, as set forth in claim 6, including at least one clamping diode coupled between the output terminal and the second terminal of the voltage supply.

ABSTRACT OF THE DISCLOSURE

A logic gate includes a low noise current source coupled between a first terminal of a voltage supply and an output terminal. The low noise current source is capable of delivering a preselected voltage signal to the output terminal having a magnitude responsive to a first control signal relatively independent of the magnitude of the voltage on said first terminal of said voltage supply. At least one switching element is coupled between the output terminal and a second terminal of the voltage supply. The switching element is capable of coupling the output terminal to the second terminal of the voltage supply in response to receiving a second control signal.

FIGURE 1

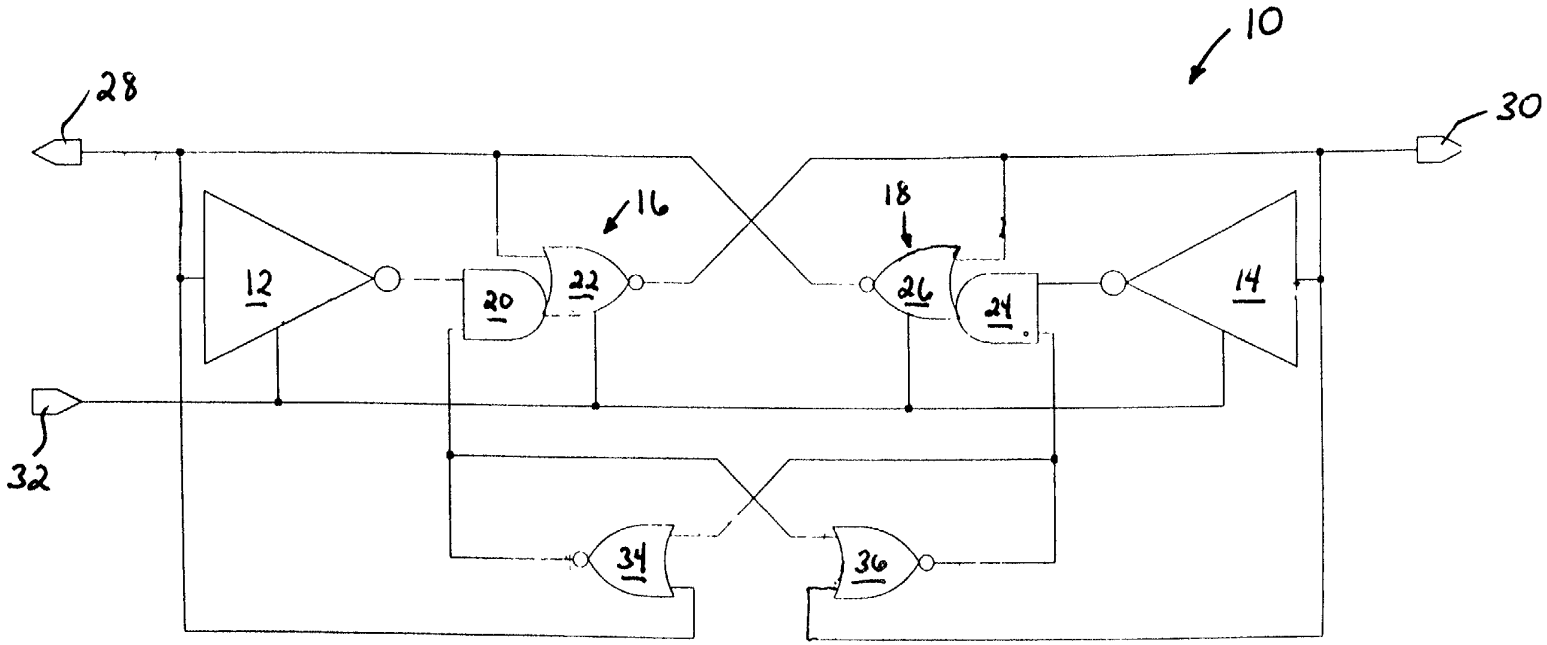


FIGURE 2

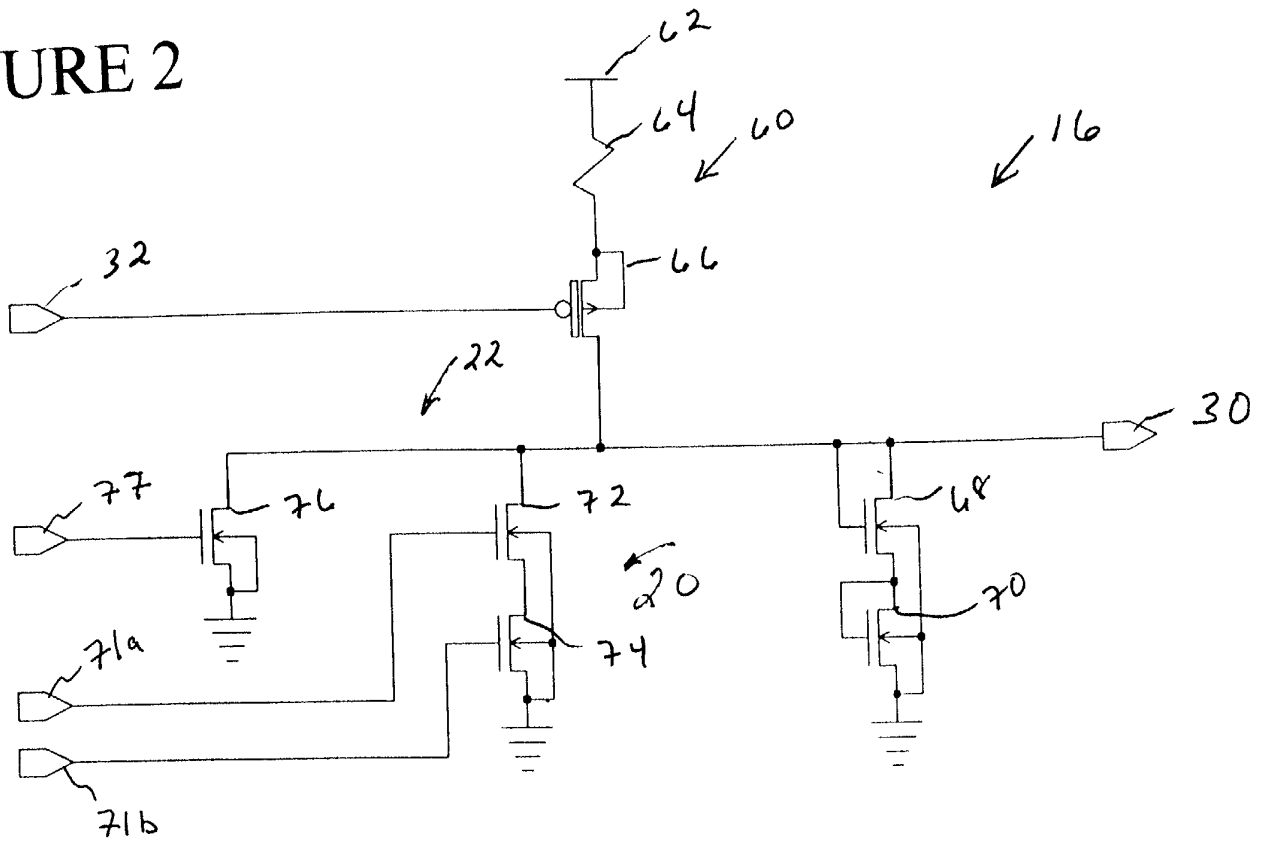


FIGURE 3

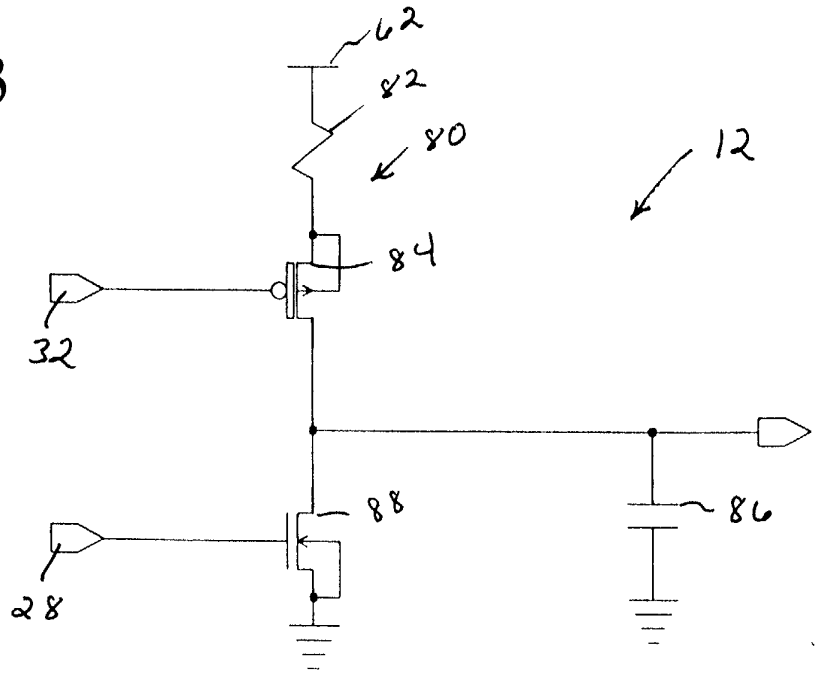
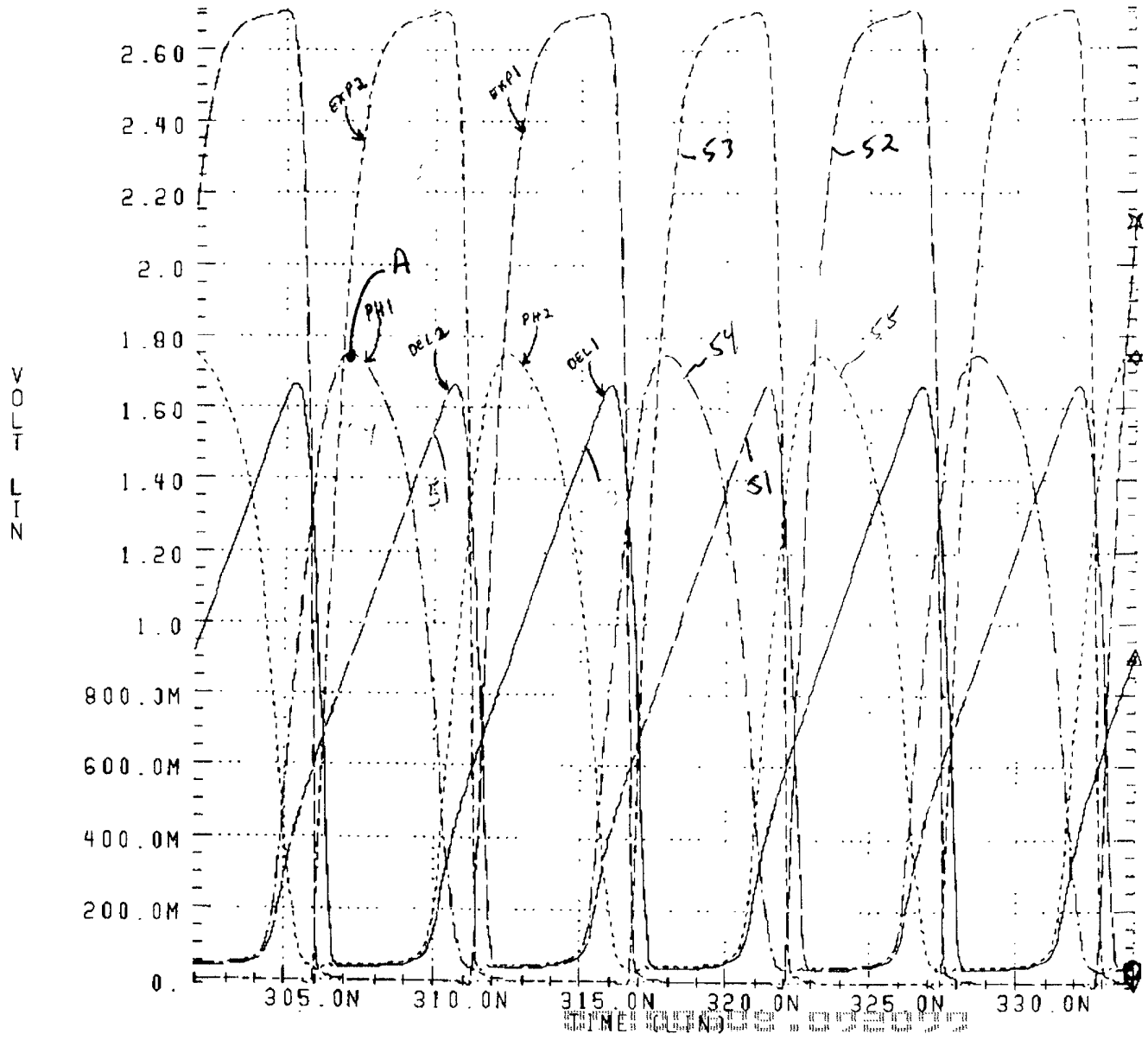


FIGURE 4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S2
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S5

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TT2273

DECLARATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or the below named inventors are the original, first and joint inventors (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention **LOW NOISE LOGIC GATES**, the Specification of which:

☒ is attached hereto.
☐ was filed on as Application Serial No. .

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent, United States provisional application(s), or inventor's certificate listed below and have also identified below any foreign application for patent, United States provisional application, or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIORITY APPLICATION(S)			Priority Claimed
(Number)	(Country)	(Date Filed)	Yes/No
(Number)	(Country)	(Date Filed)	Yes/No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations, § 1.56, which become available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status)
(Application Serial No.)	(Filing Date)	(Status)

I hereby direct that all correspondence and telephone calls be addressed to Terry D. Morgan, Williams, Morgan & Amerson, P.C., 7676 Hillmont, Suite 250, Houston, Texas 77040, (713) 934-7000.

I HEREBY DECLARE THAT ALL STATEMENTS MADE OF MY OWN KNOWLEDGE ARE TRUE AND THAT ALL STATEMENTS MADE ON INFORMATION AND BELIEF ARE BELIEVED TO BE TRUE; AND FURTHER THAT THESE STATEMENTS WERE MADE WITH THE KNOWLEDGE THAT WILLFUL FALSE STATEMENTS AND THE LIKE SO MADE ARE PUNISHABLE BY FINE OR IMPRISONMENT, OR BOTH, UNDER SECTION 1001 OF TITLE 18 OF THE UNITED STATES CODE AND THAT SUCH WILLFUL FALSE STATEMENTS MAY JEOPARDIZE THE VALIDITY OF THE APPLICATION OR ANY PATENT ISSUED THEREON.

Inventor's Full Name: Daren Allee

Inventor's Signature: Daren Allee

Country of Citizenship: U.S.A. Date: 9-16-98

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Austin, Tx 78758

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	§	
DAREN ALLEE	§	
	§	Examiner: Unknown
Serial No.: Unknown	§	
	§	Group Art Unit: Unknown
Filed: Concurrently Herewith	§	
	§	Atty. Docket: 2000.00900/TDM
For: LOW NOISE LOGIC GATES	§	
	§	
	§	

POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The undersigned, being the inventor named in the above-identified application, hereby revoke any previous Powers of Attorney and appoint:

> Paul S. Drake, Reg. No. 33,491; J. Vincent Tortolano, Reg. No. 31,433; Louise K. Miller, Reg. No. 36,609; Elizabeth A. Apperley, Reg. No. 36,428; Vincenzo D. Pitruzella, Reg. No. 28,656 Louis A. Riley, Reg. No. 39,817; Rita M. Wisor, Reg. No. 41,382; Charles Quarton, Reg. No. 24,825; and Richard J. Roddy, Reg. No. 27,688; of Advanced Micro Devices, Inc.; and Danny L, Williams, Reg. No. 31,892; Terry D. Morgan, Reg. No, 31,181; J. Mike Amerson, Reg. No. 35,426; Scott F. Diring, Reg. No. 35,119; of Williams, Morgan & Amerson;

as its attorney or agent so long as they remain with such firms, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive any Letters Patent, and for one year after issuance of such Letters Patent to file any request for a certificate of correction that may be deemed appropriate.

Please direct all communications as follows:

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Signature: Daren Allee Date: 9-16-99
Name: Daren Allee